(RRAIVI), a spin transfer torque random access memory (STTRAM), a magnetic random access memory (MRAM), and so on, which have a nonvolatile characteristic.

[0118] Features in the above examples of electronic devices or systems in FIGS. **4-8** based on the memory devices disclosed in this document may be implemented in various devices, systems or applications. Some examples include mobile phones or other portable communication devices, tablet computers, notebook or laptop computers, game machines, smart TV sets, TV set top boxes, multimedia servers, digital cameras with or without wireless communication functions, wrist watches or other wearable devices with wireless communication capabilities.

[0119] While this patent document contains many specifics, these should not be construed as limitations on the scope of any invention or of what may be claimed, but rather as descriptions of features that may be specific to particular embodiments of particular inventions. Certain features that are described in this patent document in the context of separate embodiments can also be implemented in combination in a single embodiment. Conversely, various features that are described in the context of a single embodiment can also be implemented in multiple embodiments separately or in any suitable subcombination. Moreover, although features may be described above as acting in certain combinations and even initially claimed as such, one or more features from a claimed combination can in some cases be excised from the combination, and the claimed combination may be directed to a subcombination or variation of a subcombination.

[0120] Similarly, while operations are depicted in the drawings in a particular order, this should not be understood as requiring that such operations be performed in the particular order shown or in sequential order, or that all illustrated operations be performed, to achieve desirable results. Moreover, the separation of various system components in the embodiments described in this patent document should not be understood as requiring such separation in all embodiments.

[0121] Only a few implementations and examples are described. Other implementations, enhancements and variations can be made based on what is described and illustrated in this patent document.

1-17. (canceled)

18. An electronic device with a semiconductor memory, the semiconductor memory comprising:

a substrate processed to include buried gates ;

a crystalized doped layer formed in the substrate and located between neighboring buried gates;

a landing plug formed between the neighboring buried gates over the crystalized doped layer and including a stack that includes a silicide layer and a metal layer;

an interlayer insulating layer formed over the substrate to cover the landing plug;

a lower electrode contact passing through the interlayer insulating layer and being in contact with the landing plug; and

a variable resistance element formed over the interlayer insulating layer and being in contact with the lower electrode contact.

19. The electronic device of claim **18**, wherein the silicide layer includes a titanium silicide layer.

20. The electronic device of claim **18**, wherein the metal layer includes a titanium nitride layer.

21. The electronic device of claim **18**, wherein the variable resistance element includes transitional metal oxide, metal oxide including perovskite material, phase-changing material including chalcogenide material, ferroelectric material, or ferromagnetic material, or a stack thereof.

22. The electronic device of claim **18**, the semiconductor memory further comprising:

a conductive line formed over the variable resistance element; and

an upper electrode contact coupling the conductive line to the variable resistance element.

23. The electronic device of claim **18**, wherein the crystalized doped layer includes impurities of sufficient dose to reduce the interface resistance between the substrate and the silicide layer.

24. The electronic device of claim **18**, wherein the substrate is processed to include trenches and the buried gates are formed in the trenches.

25. The electronic device of claim **18**, wherein the substrate is processed to include a recess between neighboring trenches in which the neighboring buried gates are formed, and wherein the crystalized doped layer and the landing plug are formed in the recess.

26. The electronic device according to claim **18**, further comprising a microprocessor which includes:

a control unit configured to receive a signal including a command from an outside of the microprocessor, and performs extracting, decoding of the command, or controlling input or output of a signal of the microprocessor;

an operation unit configured to perform an operation based on a result that the control unit decodes the command; and

a memory unit configured to store data for performing the operation, data corresponding to a result of performing the operation, or an address of data for which the operation is performed,

wherein the semiconductor memory unit that includes the resistance variable element is part of the memory unit in the microprocessor.

27. The electronic device according to claim **18**, further comprising a processor which includes:

a core unit configured to perform, based on a command inputted from an outside of the processor, an operation corresponding to the command, by using data;

a cache memory unit configured to store data for performing the operation, data corresponding to a result of performing the operation, or an address of data for which the operation is performed; and

a bus interface connected between the core unit and the cache memory unit, and configured to transmit data between the core unit and the cache memory unit,

wherein the semiconductor memory unit that includes the resistance variable element is part of the cache memory unit in the processor.

28. The electronic device according to claim **18**, further comprising a processing system which includes:

a processor configured to decode a command received by the processor and control an operation for information based on a result of decoding the command;

an auxiliary memory device configured to store a program for decoding the command and the information;

a main memory device configured to call and store the program and the information from the auxiliary